ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

LNA CASCODE WITH CURRENT REUSE FOR WLAN

Suraj N. Rathod *

* Electronic and Telecommunication , MIT Institute Of Technology, Pune, INDIA

ABSTRACT

This paper include common gate (CG) LNA for ultra wideband (UWB) applications with CMOS trans conductance "gm" boosted. Noise distortion cancelled out by gm boosting technique and power minimization with help of current reuse technique. By CG-CS topology utilized to get more efficient parameters such as gain, stability, linearity and power dissipation. This design 0.13 um process CMOS technology which operated from 2 to 5 GHz with 1v supply. The common gate LNA design achieved forward gain (S21) of 15.50 db and reverse isolation (S12) in the range -47.59 db to -42.53 db and with input return loss (S11) and output return loss (S22) are -18.50 db and -11.42 db at 3.02 GHz and 5.01 GHz frequency range intensively Noise figure improved in this paper up to 2.93 db.

KEYWORDS: common gate (CG); current reuse; ultra wideband amplifier (UWB); common source (CS); low-noise amplifier (LNA).

INTRODUCTION

In recent years, wideband applications such as software radio, millimeter wave, ultra wideband (UWB) has attracted a tremendous attention. This is mostly due to the emergence of CMOS component's implementation for such application. For this a high operating frequency and high gain amplifier need to be designed. A low noise amplifier with high matching ability and very small gain variation is best suited for this type of communication system. The demand for ultra-wide band systems has increased. These systems are a new wireless technology, which have the ability to send data over a wide bandof frequency [1]. The advantages of this technology include high data rate, low power, reduced interference and low-cost, that are critical for broadband wireless communication. An UWB LNA is a first block in an ultra-wide band transceiver and Its performance can affect the overall performance of the transceiver. The UWB LNA must be able to provide several basic requirements, such as broadband input matching, low noise figure (NF), sufficient gain to reduce the noise of the mixer, small die area and low power consumption. Ultra wideband (UWB) has attracted a tremendous attention. In the short range wireless transmission Ultra wideband (UWB) system realize high data rate, which suitable for integration in various consumer electronics such as PCS, cellular phones, PDA and digital cameras [3]. This is mostly due to the emergence of CMOS components implementation for such application [2].

For this a high operating frequency and high gain amplifier need to be designed. In the receiving chain one of the most critical block of such ultra wideband (UWB) system is the low noise amplifier (LNA). A low noise amplifier with high matching ability and very small gain variation is best suited for this type of communication system. The demand for ultra-wide band systems has increased. These systems are a new wireless technology, which have the ability to send data over a wide spectrum of frequency bands [4]. The advantages of this technology include high data rate, low power, reduced interference and low-cost that are critical for broadband wireless communication. An UWB LNA is a first block in an ultra-wide band transceiver and its performance can affect the overall performance of the transceiver. The UWB LNA must be able to provide several basic requirements, such as broadband input matching, low noise figure (NF), sufficient gain to reduce the noise of the mixer, small die area and low power consumption.

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

In the recent year CMOS UWB radio receiver front-end LNA has plays an important role. Several techniques have been reported in published literature In [5] CMOS UWB LNA architecture can divided major group's namely common gate (CG) and common source (CS). This shown in Fig. 1(a) for the common source LNA input given to the gate of transistor through the inductor and capacitor. The noise factor of CS LNA is linear with operating angular frequency and it will large in gigahertz range. In [7] difficulties due presence of parasitic capacitances. So Advanced design techniques which providing wideband input match to meet UWB matching requirement [2]. Other hand the Cg LNA is almost independent of angular frequency (W) and remains constant irrespective of the bandwidth and with frequency operation. In CG topology it relatively simple than CS achieving wideband input matching by absorbing parasitic capacitances. In Fig.1 (b) CG UWB LNA shown, it has parallel resonant with resistor, inductor, capacitor (RLC) network. It ignoring parasitic capacitance and body effect. In case quality factor Q, is given in equationally Q=WCgsRs/2 as Q is proposition to gate source capacitance (Cgs). It will help for decrease with shrinking technology and hence clear bandwidth for broadband behavior. Therefore CG LNA easily adopted for matching broadband impedance without adding extra components. In related Noise figure it depends on the device and process parameter it will remains almost constant with angular frequency (w) another way that NF of CG LNA strong coupled with biased point or 1/gm input matching resistor. It directly giving relation that if gm boosted of CMOS transistor then it will help out to reduce down NF. For more advantages use of Fig.1 (c) structure CG-CS topology. In that input given to both gate and source for CS and CG transistor CMOS topology. It help to further decreased down NF and power dissipation [1].

This paper proposed release this trade-off in the CG LNA a noise-cancelling technique [2] has been widely used. It will have operating frequency range from 2.3 to 2.6 GHz. The design main focus on the improvement of three major parameters gain, bandwidth, noise figure and they changes will gain up to 14.7 db, Noise figure up to 4.8 db. With supply voltage 1.2 v power supply to provide sufficient gain at this range a Cg-Cs cascade technique is used. This stabilizes the gain over the wide range of frequency. The current reuse technique also helps to reduce complexity and on-chip area of LNA. It also improves the noise figure and linearity. The power consumption of the device may also get reduced. We utilize g_m-boosting stage to cancel the noise of the input matching transistor it also improves the noise figure and linearity. The power consumption of the device may also get reduced. Thus with the help of this design we can obtain an LNA that has excellent performance over higher frequency region like Bluetooth, WIMAX and Wi-Fi.

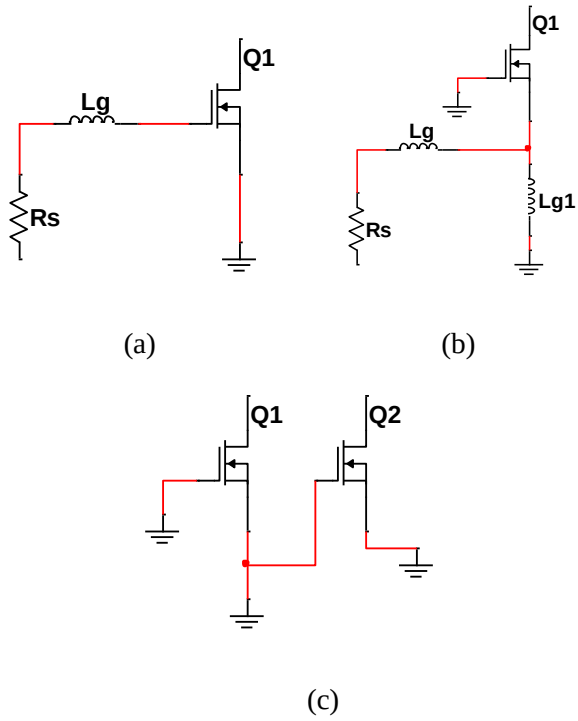

Fig. 1. CG LNA topology (a) Single common source LNA topology. (b) Common gate LNA topology (c) CG–CS topology.

Cg lna with current–reuse gm boosted

There many literature has been passed on the cascade of CS stage current. For better isolate in single inductor in [4]. LC network provide third isolation operating along with improved noise performance. In [12] same gm boosted CG LNA with current reuse technique in cascade stage (CG-CS) to boost the gain. There design has provide using transformer coil across the source and gate terminal of the input terminal of

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

device. By continuation with transformer being passive device which not consuming electric power but due to taking that it leed to nonlinearities, low resistance and causes to produced noise at output of amplifier. In they were use gm boosted technique not current reuse which utilize the active PMOS CS device for providing inverting gm boosted gain. It means they has separately biased and biased current which doesn't sharing between common gate and common source leads to more power dissipation. This paper has advantages of current reuse technique to CS which help to provide biased current in between CS-CG topology means current reuse in between them provided that power dissipation less through circuit. Also for noise cancellation gm boosted technique thus new approach here called "gm boosting current reused".

PROPOSED CG LNA WITH CURRENT REUSE

Figure:

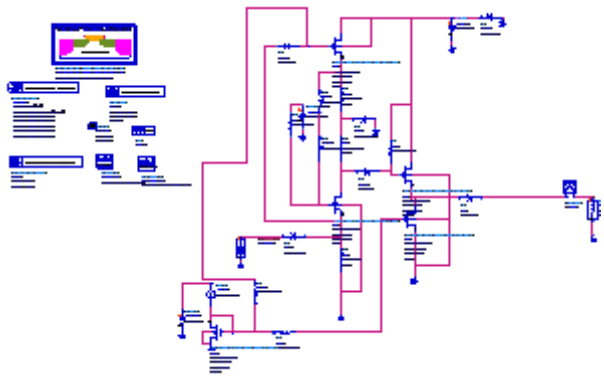

Fig. 2 Proposed CG LNA with current reuse

In the proposed circuit was carried out using ADS design tool in that design simulation was done and design of CMOS UWB LNA which based on 130 um RF CMOS process. From Fig. (2) M1 transistor used CG amplify device. For providing proper isolation between Cg and CS use tank circuit with inductor and capacitors. There M1 transistor used as CG that amplifying device due to CG it almost independent of frequency operation. Also eliminates the Miller effect help for better isolation from the output return signal current shares between CS-CG method called current reuse help to decrease down the over dissipation between M1 and M2 [8]. CS stage M2 is conjunction with low impedance path of series resonant LC tank with inductor Lt and Capacitor Ct provide inverting gain A(w). This help for increased gain A(w) by gm boosting of initial transistor M1 then factor changes to [1+A(w)]. It increased without increase its size or biased current. In that Lt And Ct provide which connect in between gate of M1 and drain of M2 low impedance path between M1 and M2. As they formed resonant circuit which was tuned near the upper end of desired bands. In the LC network low pass network has series with inductor coil ln and along shunt capacitor Csh providing isolation between M1 and M2 [8]. By the making reuse of dc biased current through ln and lp for reducing power consumption and capacitor CVsh act as bypass capacitor for AC frequency. For testing purpose act M3 and M4 providing buffer of 50 ohm resistor [9]. For getting better result in term parameter the width of M1, M2, M3, M4 optimized. Instead of register biasing RG1, RG2, RG3, RG4 of transistor use of current source provide to all of them and use supply voltage 1V. Inductors at Ln and Lp are for providing UWB bandwidth and for obtains higher gain and bandwidth optimized the noise Lt-Ct tank multiple standards and features on a single chip.

Design Considerations:

1.To study RFIC design technique using ADS tool.

2. To implement CG LNA by using a 130 nm CMOS process.

3. To achieve high gain, low noise performance.

4. To improve output linearity.

Aim: Design the Casc ode LNA with current reuse (802.11 a, b, g) WLAN application.

SIMULATION RESULT AND DISCUSSION

LNA was designed by Agilent's Advanced design system tool that designing and simulating the circuit for checking output of design parameter like S-parameter, linearity, noise figure, gain. Company designed in TSMC (Taiwan Semiconductor Manufacturing Technology) for providing net list multiple frequency bands. A single wideband LNA shared among different standards is preferred to save power and reduce complexity. Such an LNA should achieve good impedance matching, high gain, and low noise figure (NF) across a wide frequency band. The conventional solution employs several LC-tuned LNAs to cover a dedicated small band over the desired frequency span [6]. The other extreme is a wideband LNA [10] with more flexibility and better efficiency in terms of form factor, cost and power but its

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

performance must be comparable to or even better than narrowband tuned LNAs due to concurrent reception of unfiltered multi-standard signals.

Formulae:

Proposed parameter of LNA obtained by following derivations [4].

[1] Power Gain (GA)
Gain of the circuit calculate by using following formula

$$S21 = \frac{(1+S11)\,vout}{vin} \quad (1)$$

$$= (1 + S11)\frac{v\prime out}{vin}.gm3(R0//Z0) \quad (2)$$

Where

$$\frac{v\prime out}{vin} = gm1\frac{(1-w^2LgCRH)}{x(W)}\left[(Rl + jwLl)//\frac{1}{jwCl}\right] \quad (3)$$

Z0 is the 50- source resistance.
CL is the total capacitance between the drain of the transistor
M2 and ground.S21 =0 when following condition satisfied.

$$S\ 11 = -1 \text{or} \frac{V\prime out}{vin} = 0 \quad (4)$$

S11 is the reflection coefficient at the input port.

[2] Maximum stability Gain

$$\text{Gmax stabilityGain} = \frac{[S21]}{[S12]} \quad (5)$$

It will maximum when stability condition K>1 It checking for the circuit might oscillate from the voltage variation, low or high frequency.

[3] Stability factor

$$\Delta \equiv S11\ S22 - S12\ S21 \quad (6)$$

Condition
K >1 and $\Delta < 1$ then circuit is unconditionally stable. It means circuit does not oscillate of source and load impedance. So by Rollets criteria k>1

$$K = \frac{1+[\Delta]^2-[S11]^2-[S22]^2}{2[S21][S12]} \quad (7)$$

Evaluation of S parameter over wide frequency range ensure remains greater than one all range frequency.

[4] Return loss
It will calculate how much input impedance matched to reference to reference impedance or how well output impedance is matched to load impedance in power transfer. It corresponds to the return loss at input at input port and out port. Its equation given as
Input return loss
= -S11(db)
=-20log[S11] (8)

[5] Output return loss
It means how much output impedance matched to reference impedance or how well output impedance is matched to load
Impedance in power transfer.
Its equation given as
= -S22(db)
=-20log[S22] (9)

[6] Nosie Analysis
Noise Figure calculate by using formulae
NF=10log F. (10)

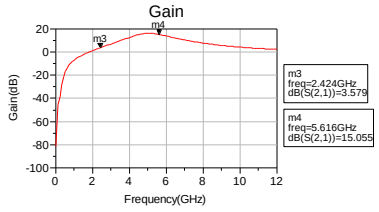

Fig. 3 (a). Simulated power gain (S_{21}) versus frequency

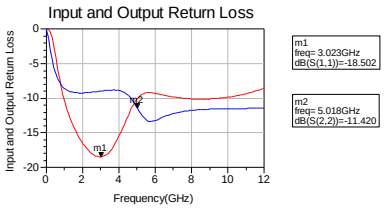

Fig. 3 (b). Simulated input return loss (S_{11}) and output return loss (S22) versus frequency.

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

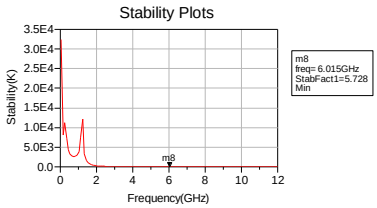

Fig.3 (c). Simulated stability factor versus frequency.

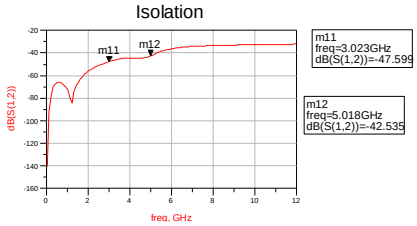

Fig. 3 (d). Simulated Isolation (S_{12}) versus frequency.

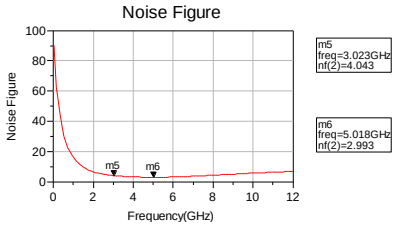

Fig. 3 (f). Simulated noise figure (NF) versus frequency.

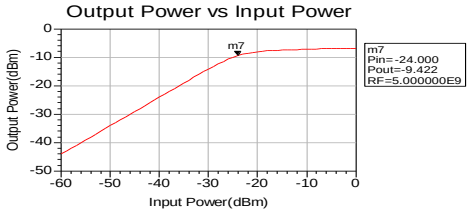

Fig .3 (g). Output power Vs input power

From figure Simulated S-parameter results are shown in fig. 3(a) to 3(g). from Fig. 3(a) shows simulated maximum power gain (S_{21}) which is 15.50 dB with 3 dB bandwidth at 5.018 GHz. It was dependent that how much S11 and S22 matched together and circuit noise. In Fig. 3(b) input and output return loss (S11 ,S22) are -18.5 db and -11.42 db at 3.02 GHz and 5.01GHz respectively. For stability check of the circuit in Fig. 3(c) at frequency 6.015 GHz got 5.72 db it was greater than 1 it means circuit not oscillate. From Fig. 3(d) reverse isolation S12 is in the range -47.595 db to -42.535 db at 3-5 GHz frequency range. In Fig. 3(f) simulated noise figure obtained 2.93 db at 5.081 GHz and also From fig 3(g) input intersect point IIP3 1.078 which improved than previous paper [1, 2, 3, 4].

Tables:

Table 1. Summary for measurement Result

Technology	130
Frequency	2-5 GHz
Parameter	Result
NF	2.93 dB
S11	-18.5dB
S22	-11.42 dB
S21	15.5 dB
S12	-47.59 dB
Power	3.3 mW
Stability	5.72 dB
IIP3	1.078 dBm

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

Table 2. Comparision with the previous paper Designs.

	This work	[1]	[2]	[3]	[4]
Technology	130	130	180	180	180
Year	2015	2012	2014	2010	2010
Frequency	2-5 GHz	3-5	2.3-2.6	3-11	3-4.8
NF	2.93 dB	3.5-4.5	4.8	4.7-5.2	3.5
S11	-18.5dB	<-8	<-18	<-10	<-9
S22	-11.42 dB	<-14	-	-	-
S21	15.5 dB	13	14.7	14	11.5
S12	-47.59 dB	<-40	-	<-65	-
Power	3.3 mW	3.4	0.58mW	30mW	2.5mW
IIP3	1.078 dBm	-6.1	2dBm	-5.3dB	-

CONCLUSION

In this paper CG LNA designed using the TSMC 130 nm RF CMOS process technology, operating 3-5 GHz UWB range. In this new approach to boost gm for reducing the noise of CG LNA by adopting current reuse technique also reduced power dissipations by sharing biased current between gm boosting and amplify stages.

The LNA achieving a gain of 15.50 db and low noise figure of 2.93 db over -3 db bandwidth with IIP3 in positive 1.078 db. Supply of 1.0 V with minimum 3.3 mW power consumption. Advantages of that topology in this paper, proposed LNA achieves comparable and even better than previous published designs, better noise figure, gain with low power supply voltage and high stability, linearity .

ACKNOWLEDGEMENTS

The authors gratefully acknowledge the support and guidance of the staff of Electronics department, MIT Institute of Technology, of Savitribai Phule Pune University.

REFERENCES

1. Muhammad Khurram and S.M Rezaul Hasan,Senior Member, IEEE A 3-5 GHz Current-Reuse gm-Boosted CG LNA for Ultra wideband in 130nm CMOS.IEEE Transactions Scale Intrgration (VlSI) System, Vol 20.No.3.March 2012.
2. Zhiqun Li,Zengqi Wang, Meng Zhang,Liang Chen A 2.4 GHz Ultra-Low-PowerCurrent Reuse CG-LNA With Active Gm-Boosting Technique. IEEE MICROWAVE And Wireless Components Letters ,Vol.24 .24,No.5 MAY 2014.
3. S. M. Rezual Hasan Senior Member, IEEE Analysis and Design of a Multistage CMOS Band-Pass Low-Noise Preamplifier for Ultra wideband RF Receiver. IEEE Transactions On Very Large Scale Integration (VLSI) System, Vol.18.No.4 .March 2010.
4. Andrea Bevilacqua, Member, IEEE, Christoph Sandner, Member, IEEE, Andrea Gerosa, Member, IEEE, and Andrea Neviani, Member, IEEE A Fully Integrated Differential CMOS LNA for 35-GHz Ultra wideband wireless Receiver. IEEE Microwave And Wireless Components Letters, Vol. 16, No. 3, March 2006.
5. C. P. Liang, P. Z. Rao, T. J. Huang, and S. J. Chung, Analysis and design of two low-power ultra-wideband CMOS low-noise amplifiers with out-band rejection, IEEE Trans. Microw. Theory Techn., vol. 58, no. 2, pp. 277286, Feb. 2010.
6. Aly Ismail and Asad A. Abidi, Fellow IEEE A 3-10-GHz Low-Noise Amplifier With Wideband LC-Ladder Matching Network IEEE Journal Of Solid Circuits,Vol. 39, No. 12, December 2004.
7. .-Y. Lee, H.-K. Park, H.-J. Chang, and T.-Y. Yun, 3.4-mW common-gate and current-reused UWB LNA, in Proc. IEEE 12th Topical Meeting Silicon Monolith. Integr. Circuit RF Syst. (SiRF), 2012, pp. 3336.
8. V. H. Le, S. K. Han, J. S. Lee, and S. G. Lee, Current-reused ultra low power, low noise LNA mixer, IEEE Microw. Wirel . Component let. vol. 19, no. 11,pp.755-757, Nov.2009.
9. M. D. Wei, S. F. Chang, and Y. C. Liu, A low-power ultra-compact CMOS LNA with shunt-resonating current-reused topology, in Proc. 3rd EMICC, 2008, pp.350353.
10. T. Taris, Y. Deval, and J. B. Begueret, Current reuse CMOS LNA for UW

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

applications, in Proc. 34th ESSCIRC, 2008, pp. 294297.
11. C.LinandT.S.Kalkur,A2.4GHzcommon-gateLNAusingon-chip differential inductor in a 018 um CMOS technology ,in proc.IEEE Conf.Elect Commun. Comp,2009,pp. 183-188
12. T. K. K. Tsang, K. Y. Lin, and M. N. E. Gamal, Design techniques of CMOS ultra-wideband amplifiers for multistandard communicationIEEE Trans. Circuits Syst. II, Expr. Briefs, vol.55, no.3,pp.214-218,Mar. 2008.
13. D. K. Shaeffer and T. H. Lee, A 1.5-V, 1.5-GHz CMOS low noise amplifier, IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 745759, june. 1997.
14. Ching-Piao Liang, Pei-Zong Rao, Tian-Jian Huang, and Shyh-Jong Chung, Senior Member, IEEE Analysis and Design of Two Low-Power Ultra-Wideband CMOS Low-Noise Amplifiers With Out-Band Rejection IEEE transaction on microwave theory and techniques, vol. 58, no. 2, February 2010.

AUTHOR BIBLIOGRAPHY

Suraj N. Rathod
Received his BE degree in Electronic and telecommunication Engineering from Kolhapur institutof technology College of Engineering, Kolhapur under Shivaji university in the year 2013. He is currently working towards his ME degree in VLSI from MIT Institute of Technology, under Savitribai Phule Pune University.